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10/814,866	03/30/2004	Christopher J. Diorio	IMPJ-0027B	5628

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,866	DIORIO ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/7/06 8/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of changes

1. Claims 1-72 are newly rejected see action below
2. Applicant has added new claim 73.

Claim Objections

Claims 1, 7, 9-11,14, 22, 24-26, 44, 46-48, 65-66, and 68-70 are objected to because of the following informalities:

Claims 1 and 14 contain the indefinite claim recitation of "capable of being".

Claims 7, 9-11, 22, 24-26, 44, 46-48, 65-66, and 68-70 contain the indefinite recitation of "may be changed".

Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-73 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-117 of copending Application No. 10/813907. Although the conflicting claims are not identical, they are not patentably distinct from each other because the electronic fuse as recited in claims 1-73 of the present invention is read on the electronic fuse as recited in claims 1-117 of copending Application No. 10/813907.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claims 1-73 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1-73 of copending Application No. 10/814868. Although the conflicting claims are not identical, they are not patentably distinct from each other because the electronic fuse as recited in claims 1-73 of the present invention is read on the programmable fuse as recited in claims 1-117 of copending Application No. 10/814868.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-6, 8, 12, 14-17, 19-21, 23, 29, 31-38, 41-43, 45, 53-54, 56-57, 59-60, 62-64, and 67 are rejected under 35 U.S.C. 102(b) as being anticipated by Shukuri (USPN 6,529,407)

With respect to claim 1, Shukuri discloses in Fig. 4, "an electronic fuse (circuit of Fig. 4) for selectively configuring a circuit (104) comprising:

a logic gate (latched inverters of 101) having an output node connected to the circuit (either 118 or 119 connected to the inputs of 104);

at least one nonvolatile memory element (112 or 113 of 101), said at least one nonvolatile memory element configured to be programmed to a memory value capable of causing the output of said logic gate to settle to one of two predetermined states as a power-up or a reset signal is applied to the fuse (the nonvolatile memories of 112 and 113 receive power up signals on lines 120 and 121 from 103, (see Figs. 5 and 6 which discloses 103 being controlled by reset and power-up detection circuits, thus its output is generated based on either a power up or a reset circuit) Furthermore, the output of 103 determines the level output the nonvolatile memory i.e. reading, writing, etc. (see Fig. 3) which causes the 101 to settle at predetermined state High or Low), the two predetermined states corresponding to different configurations of the circuit that are capable of being established based on the output of said logic gate (the logic circuit 101 outputs either a high or low to control 104, which corresponds to different configurations

of 104 (i.e. the output of 104 will be based on the outputs of 101))."

With respect to claims 2, 17, Shukuri discloses, "the electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a floating-gate transistor having a floating gate, an amount of charge on the floating gate determining said memory value (clearly 112 and 113 are floating gate transistors where the amount of charge on the floating gate determines the memory value)

With respect to claims 4,19, 41, and 62, Shukuri discloses, the electronic fuse of Claim 1, wherein said nonvolatile memory element comprises a nonvolatile memory element manufactured in a MOS fabrication process (clearly the 112 and 113 are MOS transistors, thus they are manufactured in a MOS fabrication process)

With respect to claims 5,20,42, and 63, Shukuri discloses, "the electronic fuse of Claim 2, wherein said floating-gate transistor is a MOS device (it can be seen that 112 and 113 are NMOS transistors)."

With respect to claims 6, 21, 43, and 64 Shukuri discloses, the electronic fuse of Claim 1, wherein said nonvolatile memory element uses a mechanism selected from the group consisting of: magnetoresistive, ferroelectric, phase-change, and dielectric, for nonvolatile information storage (clearly the nonvolatile memory of Shukuri is composed of gate insulating film, which creates a dielectric between the gate plate of the transistors, thus Shukuri discloses dielectric storage (i.e. insulation between gate plates corresponds to a dielectric)."

With respect to claims 8, 23, 45, and 67, Shukuri discloses, the floating gate transistors are programmed using hot-electron injection (see Col. 5 lines 47-52).

With respect to clam 14 Shukuri discloses in Fig. 4, "a master-slave electronic fuse for selectively configuring a circuit comprising:

"a master fuse (101) having a master latch (inverters of 101 comprise a cross coupled inverter latch) and a nonvolatile memory element coupled between (112, 113, 101 is a nonvolatile memory element see Fig. 1) a reset node (120 and 121 (output of 103)) of the master-slave electronic fuse and the master latch (112 and 113 are coupled between the reset node); and

a slave latch (104) having a slave-latch input coupled to an output of the master latch and a slave-latch node configured to receive a slave-latch signal (118 and 119 are the outputs of the master latch and are input to the input of the NOR gates of the slave latch)

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node (101 outputs at 118 and 119 are configured to settle at a high or low level according to the level at the reset node of 120 output by 103. Furthermore the output of 101 controls the input of 104, thus controlling the output of 104)."

With respect to claim 15, Shukuri discloses, "the master-slave electronic fuse of Claim 14, wherein the predetermined state of said master latch is affected by a memory value to which the nonvolatile memory element is programmed (clearly the output state of 101 is affected by the memory value to which 112 and 113 are programmed to)."

With respect to claim 16, Shukuri discloses, "the master-slave electronic fuse of Claim 15, wherein said master latch comprises cross-coupled inverters (clearly 101 is composed of cross coupled inverters)."

With respect to claims 29, 54 and 72 Shukuri discloses, "the master slave electronic fuse of claim 17, wherein the master latch is predisposed to settle into said first sate when a voltage of said floating gate is relatively high and into said second state when the floating gate voltage is relatively low (The charge on the floating gate of 112 and 113 dictates the programmed state of the nonvolatile memory, which in turn will be used to program master latch 104's output to complementary voltages on lines 118 and 119. Each programming state corresponds to a high threshold voltage (i.e. writing stage) and a low threshold (i.e. erasing state) of the nonvolatile memories. (See Col. 10 lines 3-21 and Figs. 3 and 4))."

With respect to claim 31, 56, Shukuri discloses, "the master-slave electronic fuse of claim 29, wherein said master latch comprises cross-coupled inverters (110 with 112 and 111 with 113 of 101 comprise a cross coupled latches) and wherein a first one of the cross-coupled inverters has at least one transistor with a gate-width-to-length ratio that is larger than a gate-width-to- length ratio of at least one of the transistors of a second one of said cross-coupled inverters (clearly due to the thick gate composition of 112 and 113 the width to length ratio of 112 and 113 is larger than that of 110 and 110)."

With respect to claim 32, 57, Shukuri discloses, "the master-slave electronic fuse of claim 29, wherein said master latch comprises cross-coupled inverters and wherein a

first one of the cross-coupled inverters has at least one transistor with a channel doping level that is different from a channel doping level of at least one of the transistors of a second one of said cross-coupled inverters (clearly the inverters of 101 have different transistor sizes. Thus, the smaller gate width PMOS transistors would require less doping than larger gate width NMOS transistors. Therefore, The NMOS transistors of 101 would require a larger doping level than the PMOS transistors)."

With respect to claim 33, Shukuri discloses, in Fig. 4, "a master-slave electronic fuse, comprising:

a master fuse (101) having a master latch (101 is a master latch) and a nonvolatile memory element (112) coupled between a reset node (121) of the master-slave electronic fuse and a first node of a master latch (node connected to drain of 112), and a second nonvolatile memory element (113) coupled between the reset node (121) and a second node (node connected to the drain of 113).

a slave latch (104) having a slave-latch input coupled to an output of the master latch (104's inputs are coupled to the outputs at 118 and 119) and a slave-latch node configured to receive a slave-latch signal (the input nodes of the slave latch receives the slave-latch signal output from 101),

wherein said master latch is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the master latch upon application of a slave-latch signal to the slave-latch node (101 outputs at 118 and 119 are configured to settle at a high or low level according to the level at the reset node of

120 output by 103. Furthermore the output of 101 controls the input of 104, thus controlling the output of 104)."

With respect to claim 34, Shukuri discloses, "the master-slave electronic fuse of Claim 33, wherein the predetermined state of said master latch is affected by a reset memory value associated with the first nonvolatile memory element (clearly, the predetermined state of the master latch is affected by the reset memory value associated within 112 see Fig. 3, Fig. 4 and Col. 10 lines 3-21)."

With respect to claims 35, and 59, Shukuri discloses, "the master-slave electronic fuse of Claim 33, wherein the predetermined state of said master latch is affected by a reset memory value associated with the second nonvolatile memory element (clearly, the predetermined state of the master latch is affected by the reset memory value associated within 113 see Fig. 3, Fig. 4 and Col. 10 lines 3-21)."

With respect to claims 36, and 60, Shukuri discloses, "the master-slave electronic fuse of Claim 34, wherein said nonvolatile memory element comprises a first floating gate transistor having a first floating gate, an amount of charge on the first floating gate determining said memory value (again, clearly the predetermined state of the master latch is affected by the reset memory value associated within 112 and 113 see Fig. 3, Fig. 4 and Col. 10 lines 3-21)

With respect to claim 37, Shukuri discloses, "the master-slave electronic fuse of Claim 35, wherein said nonvolatile memory element comprises a second floating gate transistor having a second floating gate, an amount of charge on the second floating gate determining said memory value (112 and 113 are both composed of the circuit of

Fig. 4, which has a floating gate transistor, and its programmed value is determined by the amount of charge present at its floating gate)."

With respect to claim 38, Shukuri discloses, "the master-slave electronic fuse of claim 35, wherein said first nonvolatile memory element comprises a first floating-gate transistor having a first floating gate, an amount of charge on the first floating gate determining said first memory value and wherein said second nonvolatile memory element comprises a second floating-gate transistor having a second floating gate, and amount of charge on the second floating gate determining said second memory value (112 and 113 are both composed of the circuit of Fig. 4, which has a floating gate transistor, and its programmed value is determined by the amount of charge present at its floating gate)."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 13, 18, 27, 39-40, 49-50, 58, 61, 71, and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shukuri in view of Goetting et al. (USPN 5,912,937) (hereinafter Goetting)

With respect to claim 3, 13, 18, 27, 39-40, 49-50, 58, 61, 71, and 73 Shukuri discloses in Fig. 4, "the electronic fuse of circuits as claimed in the rejections above

comprising a first and second nonvolatile memory circuits composed of floating gate transistors (112 and 113). Shukuri fails to disclose the first and second nonvolatile memory elements further comprises a capacitor having a first plate in common with the floating gate of said floating-gate transistor. However, it is notoriously well-known in the art that floating gate transistors a composed of a capacitor having a first plate in common with the floating gate of the nonvolatile memory transistor. This is further evidenced, in Fig. 1 of Goetting, which discloses a nonvolatile memory transistor which has "a first capacitor having a first plate (gate of 101) in common with the floating gate (FG) of said floating-gate transistor (102)." Goetting's capacitor allows for isolation between the gate and the substrate of the transistor allowing for stable programming of the transistor.

Therefore it would have been prima facie obvious for one of ordinary skill in the art at the time of the invention to use the specific floating gate transistor of Fig. 1 of Goetting in place of the generic floating gate transistors of 112 and 113 of Shukuri for the purpose of having a floating gate transistor to increase the isolation of the floating gate transistors 112 and 113. One would have been motivated to use the specific floating gate transistor of Fig. 1 of Goetting in place of the generic floating gate transistors of 112 and 113 of Shukuri to increase isolation in the transistors of Shukuri to maintain a stable programmed voltage. Thus the above combination discloses all the claim limitations of claims 3, 13, 18, 27, 39-40, 49-50, 61, 71.

With respect to clam 58 Shukuri as modified above discloses in Fig. 4, a circuit comprising:

"a master fuse (101) having a logic gate element (inverters of 101) with a reset node (120 or 121) and a nonvolatile memory element (112 or 113) comprising a MOSFET having a floating gate (112 or 113) configured to receive charge by way of hot-electron injection (112 and 113 receive charge by way of hot-electron injection, see Col. 5 lines 47-52), and further comprising a tunneling capacitor sharing said floating gates as a capacitor plate which is configured to lose charge by way of tunneling (as modified above 112, and 113 contain the capacitor of 101 of Fig. 1 of Goetting, which loses charge by way of tunneling); and

a slave latch (104) having a slave-latch input coupled to an output of the master fuse (104's inputs are coupled to the outputs at 118 and 119) and a slave-latch node configured to receive a slave-latch signal (the input nodes of the slave latch receives the slave-latch signal output from 101),

wherein said logic-gate element is configured to settle to a predetermined one of a first state and a second state following application of a reset signal to the reset node, and the slave latch is configured to latch the predetermined state of the logic-gate element upon application of a slave-latch signal to the slave-latch node (101 outputs at 118 and 119 are configured to settle at a high or low level according to the level at the reset node of 120 output by 103. Furthermore the output of 101 controls the input of 104, thus controlling the output of 104)."

With respect to claim 73, clearly Shukuri teaches the circuit as recited in claim 33, and as can be seen in the rejection of 58 above, the combination of Shukuri and

Goetting discloses the nonvolatile memory being programmed by hot-election injection and further including a tunneling capacitor.

Claims 7, 9-11, 22, 24-26, 44, 46-48, 65-66, and 68-70 are rejected under 35 U.S.C. 103(a) as being unpatentable Shukuri (USPN 6,529,407) in view of Madurawe (USPAPN 2005/0149896).

With respect to claims 7, 9-11, 22, 24-26, 44, 46-48, 65-66, and 68-70, Shukuri discloses the nonvolatile memory 112 and 113 being programmed by hot-electron injection. Shukuri does not disclose the floating gate transistors of 112, 113 being programmed by Fowler-Nordheim tunneling, direct tunneling, ultraviolet radiation exposure, etc. However, it is notoriously well-known in the art that all of the recited programming are known programming procedures and a nonvolatile floating gate transistor can be programmed by any of the recited procedures of claims 7, 9-11, 22, 24-26, 44, 46-48, 65-66, and 68-70. This is further evidenced in lines 20-21 paragraph [010] of Madurawe, which discloses the choice of the above programming techniques are chosen from user to user. Furthermore, Madurawe discloses all of the recited programming techniques of claims 7, 9-11, 22, 24-26, 44, 46-48, 65-66, and 68-70 in paragraph [0010] and that they are well-known in the art.

Therefore it would have been prima facie obvious to one of ordinary skill in the art to use any of the disclosed programming techniques as disclosed in paragraph [0010] of Madurawe to program the floating gate transistors 112 and 112 of Shukuri depending upon a desired application or a particular environment of use, the selection of a particular process of steps of programming the nonvolatile memory would have been

performed to ensure an optimal performance of the circuit. Furthermore, such a provision of selecting specific steps and timing involves only routine design expedient. Thus the above combinations of the teachings of Shukuri and Madurawe disclose all of the claim limitations of claims 7, 9-11, 22, 24-26, 44, 46-48, 65-66, and 68-70

Claims 28, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shukuri (USPN 5,912,937) in view of Pascucci et al (5,659,498). Shukuri teaches the circuits of claims 14, and 29 (see above rejections). Shukuri does not teach the required capacitor and latch output connections. However, Pascucci et al. teaches, in Fig. 1, a latch circuit with capacitors (13, 12) attached to the outputs of a cross-coupled inverter latch and fixed voltages. Pascucci et al.'s is a latch used in a fused circuit to further reduce the possibility of accidental programming and has reduced power consumption when the fuse has not yet been programmed.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the un balanced cross-coupled inverter latch of Pascucci et al., in place of the cross coupled inverter latch 101 of Shukuri for the purpose of having a latch capable of preventing a false program, and has reduced power consumption. One skilled in the art would have been motivated to use Pascucci et al.'s latch of Fig. 1 in place of Shukuri's latch 101 to lessen power consumption, and the chance of a false programming occurrence in Shukuri's circuit of Fig. 4.

With respect to claim 28, the above combination discloses, "the master-slave electronic fuse of claim 14, further comprising a capacitive element coupled to an output of the master latch (101 as modified above has a capacitor 12, or 13 coupled to an

output node 118 or 119.)."

With respect to claim 30, the above combination discloses, "the master-slave electronic fuse of claim 29, further comprising a capacitive element coupled between an output of the master latch and a fixed voltage source. (latch 101, as modified above, element 13 is a capacitor coupled to output 118 and voltage source Vdd. Additionally, 12 is also a capacitor coupled to output 119 and voltage source ground.)"

Claims 51-53 and 55, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shukuri (USPN 6,529,407) in view of Hartgring et al. (5,086,331). Shukuri teaches the circuit of claim 38, and 54 (see above rejections). Shukuri does not teach the required capacitor and latch output connections. However, Hartgring et al. teaches, in Fig. 3, a latch circuit with capacitors (Cp, Cout) attached to the outputs of a cross-coupled inverter latch and fixed voltages. Hartgring et al.'s is a latch allows for the use of smaller transistors.

It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to use the latch of Hartgring et al., in place of the latch 10 of Shukuri to reduce the size of the transistors used in Shukuri's circuit. One skilled in the art would have been motivated to use Hartgring et al.'s latch of Fig. 1 in place of Shukuri et al.'s latch 101 to obtain an efficient packaging of the transistors, and thus an efficient chip deign of Shukuri circuit.

With respect to claim 51, the above combination discloses, "the master-slave latch of claim 38, wherein a first output of said master latch is capacitively coupled to a first source of a fixed voltage (in modified latch 101 element Cp is a capacitor coupled to

output 118 and voltage source ground)."

With respect to claim 52, the above combination discloses, "the master-slave latch of claim 51, wherein a second output of said master latch is capacitively coupled to a second source of a fixed voltage (in modified latch 101 element Cout is a capacitor coupled to output 119 and voltage source ground)."

With respect to claim 53 it can be seen that both Cp and Cout are coupled to ground.

With respect to claim 55, 101 as modified above 101's outputs are coupled to the fixed voltage of ground via Cout.

Response to Arguments

Applicant's arguments with respect to claim 1-73 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
September 15, 2006

LINH MY NGUYEN
PRIMARY EXAMINER